METHOD AND APPARATUS FOR FORMING IMPROVED METAL INTERCONNECTS

This application is a continuation of United States Patent Application Serial No. 10/067,709, filed February 5, 2002, now Patent No. 6,709,987 which is a continuation of U.S. Patent No. 6,559,061, which is a continuation of United States Patent No. 6,287,977, all of which are hereby incorporated by reference herein in their entirety.

FIELD OF THE INVENTION

The present invention relates to semiconductor device metal layer interconnects and more particularly to reducing the contact resistance of interconnects.

BACKGROUND OF THE INVENTION

A typical integrated circuit contains a plurality of metal pathways to provide electrical power for powering the various semiconductor devices comprising the integrated circuit, and to allow these semiconductor devices to share/exchange electrical information. Within integrated circuits, metal layers are stacked on top of one another by using intermetal or "interlayer" dielectrics that insulate the metal layers from each other. Typically, however, each metal layer must form electrical contact to an additional metal layer. Metal-layer-to-metal-layer electrical contact is achieved by etching a hole (i.e., a via) in the interlayer dielectric that separates the first and second metal layers, and by filling the resulting hole or via with a metal to create an interconnect as described further below.

The use of copper in place of aluminum as the interconnect material for semiconductor devices has grown in popularity due to copper's lower resistivity. Unlike aluminum, however, copper is highly mobile in silicon dioxide and may, as a result of infiltration of copper atoms